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TIQ Comparator Based Performance Analysis of Pipeline Analog to Digital Converter

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ABSTRACT: High-performance analog-to-digital converter integrated circuits are in high demand because of new uses in wireless communications, broad band transceivers, digital-intermediate frequency (IF) receivers, and many other digital devices (ICs). Resolution, sampling rate, and power consumption all need to be at their best for these ICs. The goal of this research is to find a way to design a pipeline analog-to-digital converter (ADC) that uses the least amount of power and still has a good speed and resolution. In this study, a 14-bit resolution pipelined analog-to-digital converter (ADC) is built. The pipelined architecture makes it possible to get both high speed and high resolution. Pipeline ADC is used because it can make some parts of flash ADC easier to use. Calibration steps have a big effect on the absolute and relative accuracy of pipelined ADC. This paper shows an example of a 14-bit, 80-Megabit-per-second ADC made with CMOS technology and a 0.18-micrometer pitch. The converter has seven pipelined stages, and each stage uses 0.18 CMOS technology to implement two bits.

Key words: Pipe Line ADC, Amplifier, flash ADC, CMOS technology

1 INTRODUCTION

Popular among ADCs requiring resolutions of 8 to 14 bits and sampling rates between a few MS/s and hundreds of MS/s is the pipelined topology. Its popularity can be ascribed to its relatively simple and repeating interior architecture, as well as a notable reduction in the number of comparators necessary to attain a fixed resolution when compared to other Nyquist-rate data converters such as Flash, folding interpolating, etc. Mobile systems, CCD imaging, ultrasonic medical imaging, digital receivers, pedestal stations, digital video (e.g. HDTV), xDSL, cable modems, and fast Ethernet are examples of applications that utilise pipelined ADCs [1]. With the use of pipelined ADCs in several consumer items, research into enhancing the performance of pipelined ADCs has received a great deal of attention over the past decade, with linearity improvement and power reduction being the most commonly explored areas. With deeper sub-micron technology, low inherent gain, low supply voltages, and device mismatch have made it difficult to achieve extremely linear data converters (i.e., >10-bit linear) using typical pipelined ADC design. Low power consumption in pipelined ADCs is inspired by the prevalence of pipelined ADCs in mobile systems, where low power consumption permits longer battery life and consequently greater consumer efficiency. In agitated systems in which a large number of ADCs may be integrated on-chip simultaneously, enormous net supremacy expenditure might generate large amounts of heat, necessitating expensive packaging for heat dissipation. Thus, approaches that lower the power consumption of pipelined ADCs make mobile and wired integrated circuits more cost-effective. The pipelined ADC topology is utilised to derive and demonstrate an alternative approach to standard quantizes based on accurate analogue signal processing. By outsourcing various precise requirements from the analogue domain to the digital domain, the suggested converter may take advantage of the scalability of technology rather than being hampered by its constraints. In recent years, more and more system functionalities have been incorporated onto a single chip, as electronic systems have become increasingly complex and very deep submicron technology have made this possible. Therefore, mixed signal Integrated Circuits (ICs) that integrate digital and analogue components on the same substrate are widely used. Other than the extreme density

II RELATED WORK

This study presents the design of a 12-bit Pipeline Analog to Digital Converter (ADC) with a 40 MS/s sampling rate utilizing a modified Operational Amplifier (OP-AMP). The ADC design is comprised of eleven pipeline stages, including ten 1.5-bit pipelined ADC stages and one 2-bit flash ADC. This design is implemented using 90-nm CMOS technology. Various approaches, like sample and hold (SH) less design, OPAMP sharing, and capacitor size scaling in ADC pipeline stages, minimize the ADC's

power consumption. FFT analysis yields a Signal to Noise and Distortion Ratio (SNDR) of 71.22 dB, which corresponds to an Effective Number Of Bits (ENOB) of 11.53 when the sampling rate is 4 MHz. The suggested 12-bit pipeline has a power consumption of 47.3 mW and a supply voltage of 1.2 V.

Tobias Buckel et.al Combining conventional in phase and quadrature (I/Q) modulation with limited phase modulation is demonstrated to be a viable method for developing a novel digital-intensive hybrid transmitter (TX) architecture. The proposed architecture incorporates an RF-DAC with a phase-modulated RF clock and redesigned I/Q components. Through the use of phase modulation, the quadrature component can be kept to a minimum while the in-phase component grows closer and closer to the complex signal envelope. Comparing the digital-quadrature TX architecture to the RF-DAC TX architecture, the average and peak RF-DAC cell usage is significantly lower. Consequently, the RF-DAC can be operated with less back-off while maintaining increased average output power and drain efficiency. Phase modulation is restricted so that the system requirements for phase modulators can be relaxed. This results in lower frequency modulation and digital-controlled oscillator tuning range requirements compared to a digital polar TX architecture employing an RF digital phase-locked loop with two-point phase modulation. In addition, the design work is shifted from the analogue domain to the digital domain in order to make better use of the CMOS scaling benefits.

Pummy Ratna et.al . EW transceivers with a high input dynamic range, a wide bandwidth, and overlapping RF and IF frequency bands for detecting and characterising incoming signals at the same time are prone to RF and LO leakage to IF. This can cause leakage and spurs to be mistakenly identified as threat signals when traditional methods are used. This is because EW transceivers have a wide input dynamic range, overlapping RF and IF frequency bands, and a high input dynamic range. In this paper, a better architecture for a receiver is shown. For the RF part of a wideband digitally channelized transceiver, this design has been built and tested successfully. The goal of this architecture is to find threat signals as precisely as possible. To do this, the whole input frequency band is converted to X-band and then down-converted to overlapping IF. This solves the problem of direct leakage and reduces the need for image and spurious rejection filter rejection and mixer isolation. Also, it gives clean downconverted signals for Nyquist sampling at low IF in many different input situations. The system has been tested successfully with spurs, RF, and LO leakage levels of -60 dBm for closely spaced dual input pulsed signals in a dynamic range of -10 to -50 dBm. The improved architecture, the test results, and a comparison of the test results with the heterodyne architecture have all been shown.

As the throughput must be as quick as flash ADC, each stage of the pipeline ADC's structural architecture is inherited from flash. The resolution of each step will determine the number of comparators, the latency of the structure, the type of DAC architecture required, and the need for quick encoding circuitry. For example, if we select 3 bits per stage for a 7-bit pipeline ADC, there will be a total of three stages, one of which will have a one-bit ADC and the other two will have a three-bit ADC architecture; therefore, the total number of comparator required is 35(23+23+1-2), as well as two (2 bit) and one (1 bit) DAC. Since the specified architecture consists of a one-bit ADC, only one comparator is required, bringing the total number of comparators to 7. This is the impetus, which simplifies the design of other sub-blocks of each stage, such as the design of DAC and accompanying digital circuitry. Figure 1 illustrates the architecture of each pipeline ADC stage. The required components for the design of each stage of pipeline ADC (shown in Figure 1) are as follows:

- Sample and Hold.
- TIQ Comparator.
- 2-bit DAC.
- Amplifier configure for gain of 4.
- Analog Adder.
- Operational amplifier
- D flip-flop

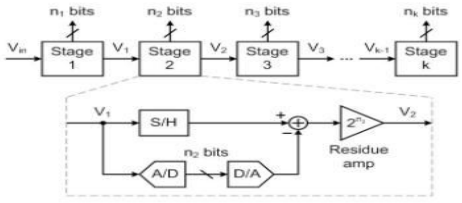


Fig1 block diagram of pipeline ADC

Design of Comparator: Implemented flash ADC uses the Threshold Inverter Quantization (TIQ) approach for low-power and high-speed ADC with standard CMOS technology. The block diagram of the Threshold inverter qunatizer comparator is depicted in Figure 2. Using cascade inverters in conjunction with a voltage comparator is the explanation for the procedure's moniker. Voltage comparators measure up to the input voltage using internal reference voltages, which are determined by the size of the inverters' transistors. A few of the most significant issues with the conventional comparator structure utilised in ADC systems are:

- large transistor area for higher accuracy,
- DC bias requirement,
- Charge injection errors,
- metastability errors,
- Resistor or capacitor array requirement.

This case, BICMOS technology would be necessary to integrate both a high-speed conversion and low-power dissipation. The proposed comparator that is described in this thesis has been developed not only for higher speed but also for higher resolution.

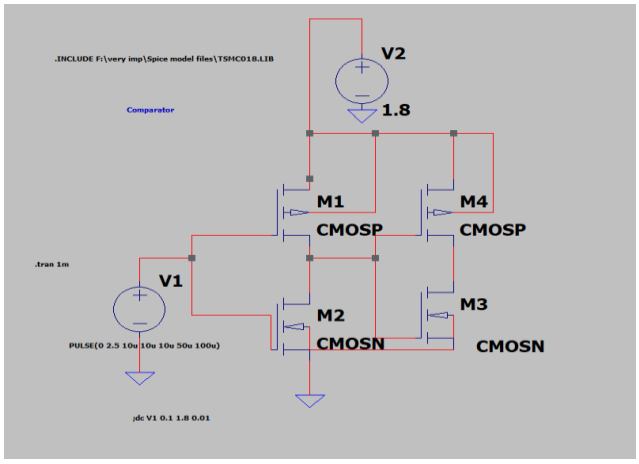
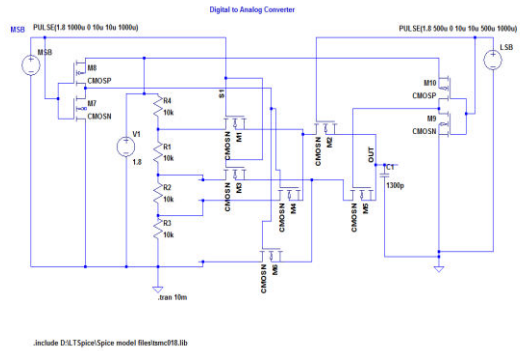


Figure 2 Schematic of Comparator

Design of Two Bit DAC: There are different configurations that can be used to design digital to analog converter (DAC) similar to resistor hierarchy (voltage separator architecture), charge division rule, current division architecture and many others, but all of this uses lot many components and complex in nature. Thus to digital CMOS technology, multiplexer logic has been employ to act as DAC, since the purpose of DAC is to provide an analog voltage corresponding to digital bits, That means a effortless analog multiplexer can do this trade The logic equation recitation the procedure of the Multiplexer that we are using here as a 2-DAC.



Which is having similar working like active ladder network the active resistor is a MOS connected in diode configuration, i.e. drain is connected to gate and source to substrate. The intend of this vigorous resistor network is reliant on the power and area restraints given. As VGS=VDS of every MOSFET, it will activate in saturation region and have set resistance.

Sample & Hold Circuit: Sample-and-hold circuitry is necessary for ADC front-end circuits to allow the ADC to track and then hold the inward bound signal. For argument of sample and hold circuitry.) Once the signal has been tracked, the ADC throws a switch to disconnect the input signal from the front end; it then holds that input signal level long enough for the ADC to complete its conversion cycle. These sample-and-hold or T/H circuits possess considerable bandwidth to allow the ADC to track high input frequencies. They must remain linear over this wideband width, which requires excellent design techniques to provide the high bandwidth without adding unnecessary noise coupling. The switch and hold capacitors must charge up and hold the signal representation for considerable times to allow the ADC quantize to accurately estimate the changing input signal amplitude

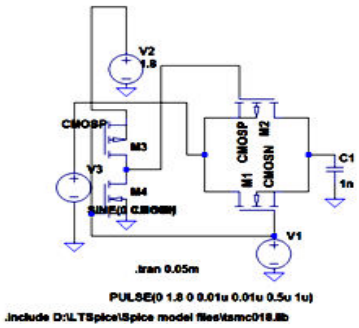


Fig 3 Schematic of 2-Bit DAC

The sampling CLK is known to the CONTr of the Tx gate. When the CLK is high the input signal is sampled from side to side the 1st buffer and the capacitor is charged to the input level. When once the CLK goes to LOW, then the path from the input is open circuited and the sampled voltage is maintain constant and given to the previous block for conversion. For a better sampling the sampling rate should be at least 2 times to that of the input gesture frequency.

Sampling Strategy: The sampling period is kept small as compared to holding period; this is kept so that the output of the OPAMP will get settled, two clocks of same period but no overlapping in nature is used one for sampling the analog voltage and other is used to latch the converted data. This method is chosen because, if the output is directly taken from the comparator .the output of ADC will oscillate and so that output of DAC which will result in cumulative error and thus a flip-flop is put in front of comparator so as to convert the settled value from S/H amplifier.

Design of D Flip-Flop: Flip-flops are the traditional storage elements used to realize synchronous logic circuits. They save the state of the machine from one clock cycle to the next. They are also used to break up any feedback loops around a cyclic logic circuit to prevent the logic from having race condition or oscillations. It is one of the necessary elements in the pipeline ADC, the main point to raise here is that, it is used as delay element which will synchronize the bits of the all stages, by configuring the flip-flop as varying length shift register, and it will synchronize the output of pipeline ADC. For example for 7 bit pipeline ADC, first stage has 7 bit shift register, in the later stage it will be of length 6 and decrementing to 1 in the last stage. The other use of this flip-flop is in the end of conversion signal generation,

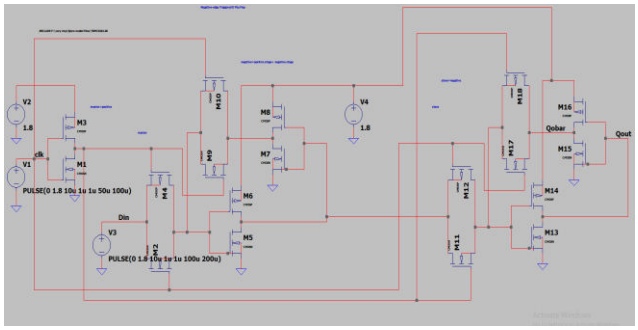


Figure 5 Schematic of D-Flip-Flop

In which it is configured as counter which will start counting when the ADC get start of conversion signal and will be stopped after counting seven clock cycles.

TC to BC Encoder: The encoder converts the 01 code to the 1 code in two ladder. The 01 code is changed to the 1-out-of-n code, by the '01' generators. This code is then converted to binary code. Shows a single cell optimized '01' generator circuit by means of only four transistors, only if full swing output in a small layout area. For the 6-bit A/D converter, 63 '01' generator cells are used in corresponding to generate 1-out-of-63 code.

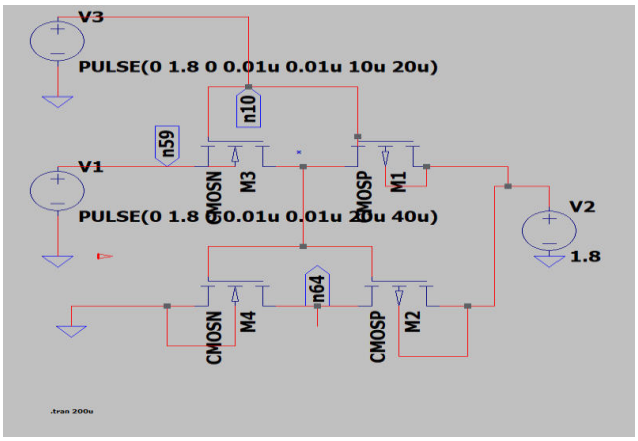


Fig 6 Schematic of TC to BC Encoder

SIMULATION RESULTS & DISCUSSION

The Threshold Inverter Quantization (TIQ) method is used to make flash ADC low-power and high-speed with standard CMOS technology. Figure 2 shows a block diagram of how the Threshold inverter quantizer comparator works. The name of the process comes from the fact that it uses cascade inverters and a voltage comparator. Voltage comparators use internal reference voltages that are set by the size of the transistors in the inverters to measure voltages up to the input voltage. Some of the biggest problems with the traditional comparator structure used in ADC systems are as follows:

Results of Sample & hold : The transient response of the sample &hold circuit shows in Figure 8

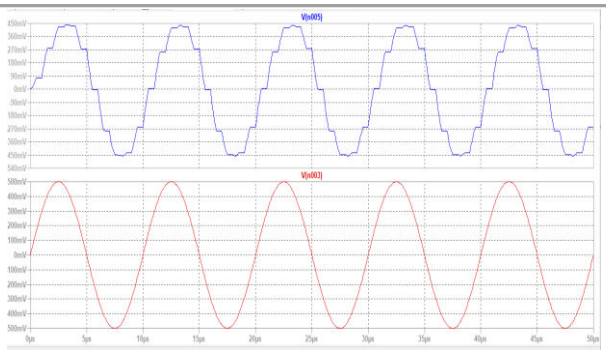


Figure 7. Transient Result of Sample & Hold Circuit

Results of Comparator: The dc breakdown result of comparator, whose reference is set at 0.9 volt. Curve shows output of the second stage .the Transient results of the comparator.

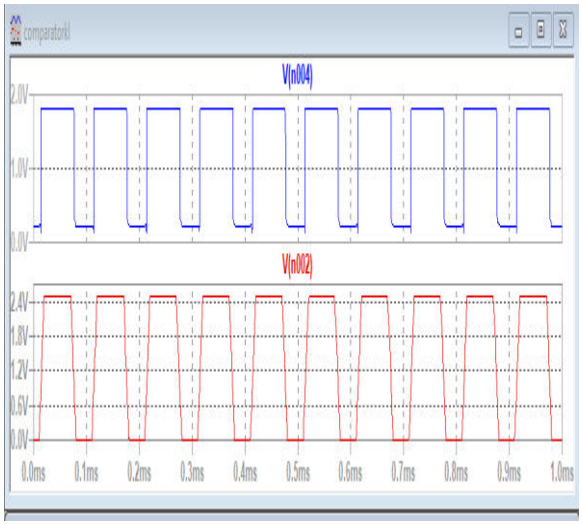


Fig 8 Transient Analysis Of Comparator

Results of DAC

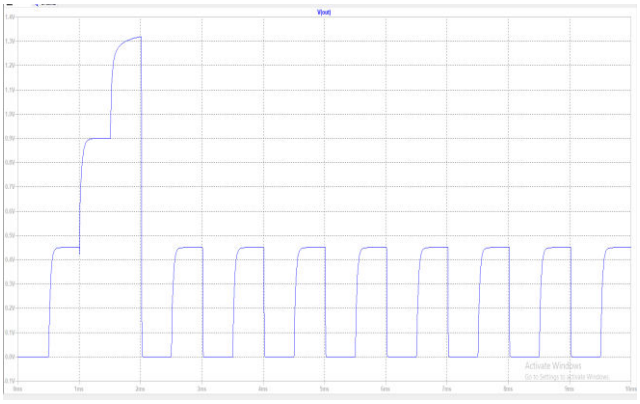


Figure 9 Transient Results Of DAC

Results of D-Flip flop

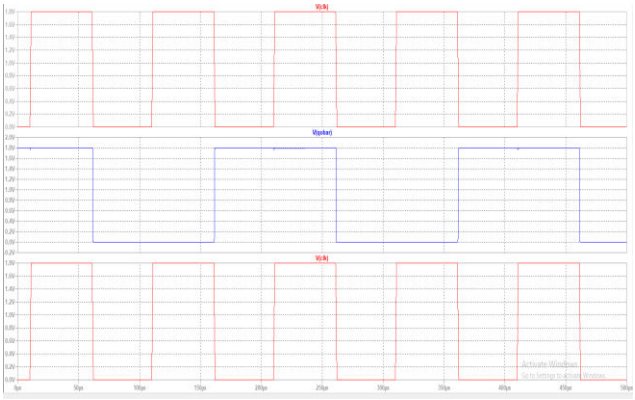


Figure 10 Transient Result of D-Flip-flop

Results of TC-T0- BC Encoder: the transient response of the tc to bc Encoder results is shown in Figure 11

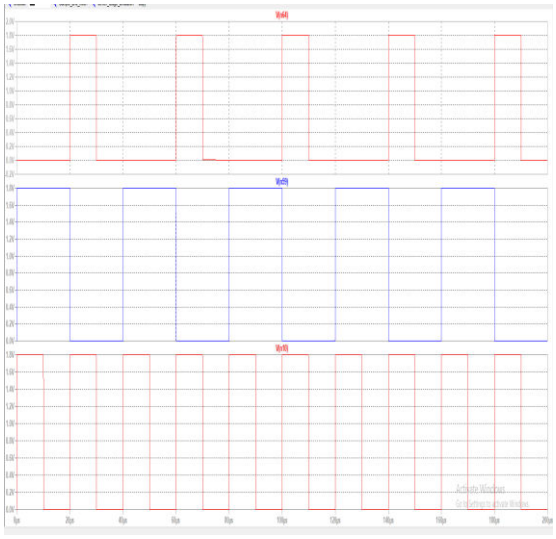


Figure 11 Transient result of TC- TO -BC Encoder

Implementation of Pipeline ADC: Here we will express how the pipelining is implementing by addition the sub - circuits those we have intended above**.** In first step **to** intend pipeline we need to design Sample & hold circuit ,2-bit ADC,2-bit DAC, An Adder and a inverting Gain amplifier. Which we have designed, here we will use six stages to get the resolution of 14-bit. When we will be suitable the input signal to Sample & hold circuit. Obtain the sampled output and these functional to comparators and get the digital output this digital signal applied to DAC unit to analog signal and output of DAC subtracted to sampled output and amplified by inverting gain amplifier, further applied to second stage.

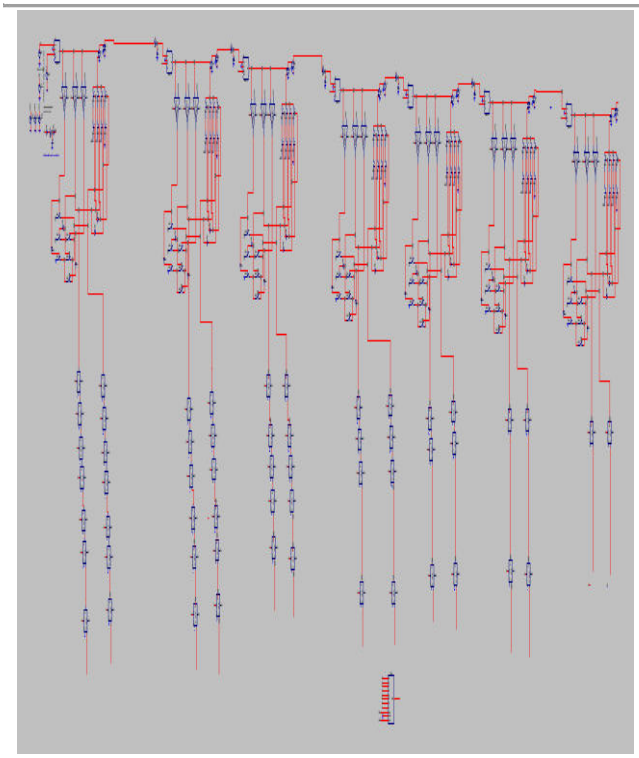


Figure 12 Schematic of 14-Bit Pipeline ADC

Results of Pipeline ADC: Presents the plot of 14-bit pipeline ADC with sinusoidal input shown in Figure 14

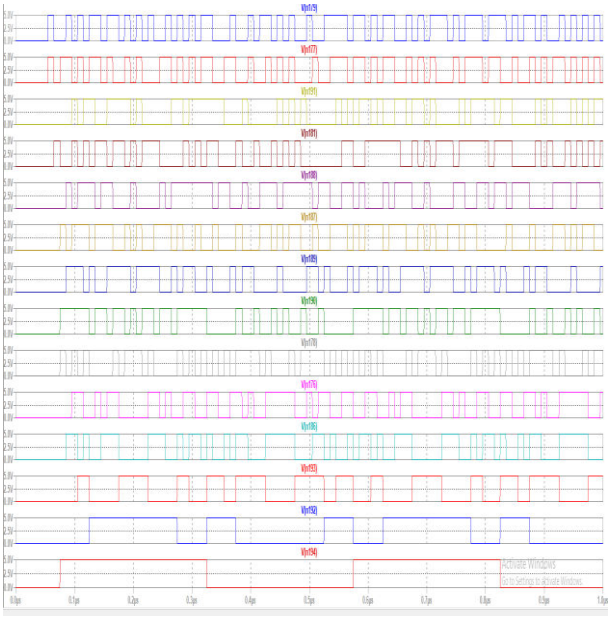


Fig 13 -14-bit pipeline ADC with sinusoidal input and output

Table 1 Comparison of the Earlier Work Done With Proposed Design Results

S.No	Name of Parameters	Earlier work done [1]	Proposed design
1	Resolution	12bit	14bit
2	Comparator	7	3
3	Sampling frequency	20MHz	40MHz
4	Power dissipation	47 mW	3.7mW
5	Gain	68dB	77dB
6	Power supply	1.8V	1.8V

CONCLUSION

The Design of 14 bit pipeline ADC has been carried out in TSMC 018µm technology. The design is implemented in LT SPICE SWICHER CAD –III Schematic Editor and the results are verified with LT spice and simulation viewed in LT SPICE. The key Design module is summarized now. 3- TIQ Comparator is worn in single stage of ADC. An Analog multiplexer is used as DAC. An OPAMP has been used in analog adder. A unity gain Inverting amplifier is Designed using an OPAMP for sample and hold circuit. An Analog adder is designed using OPAMP. Shift register has been designed using d flip-flop. The overall Design is tested with various input signals and the results are obtained satisfactory for the specification. Because of convergence problem occurring in the tool only 14 -bit design of ADC is carried out. The 14-bit pipeline ADC is working up to 1 Ghz input frequencies

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